ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

REVIEW ON THE DESIGN OF THE ALU PROCESSOR

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DOI: 10.5281/zenodo.212072

ABSTRACT

Arithmetic and logical unit are responsible for all computationally intensive task which determines the speed and reliability of a processor. In other word we can say ALU is the brain of a processor. Nowadays every portable devices are battery operated so primary concern of those devices are low power consumption. But at the same time we want higher performance also so that there should not be any lag while using those devices. Graphically intensive application demands more resources and at the same time demands more power. Optimization between speed of operation and power consumption is the key challenge in design paradigm. The performance increase can be achieved by increasing clock frequency, but it leads to some other issues such as overheating, leakage etc.

KEYWORDS: ALU, Verilog, FPGA, Artix-7, System design

INTRODUCTION

In today's advanced world, everyone wants the processor, which has low cost and power consumption. Many of the processors have high consumption of energy. There were many architectural designs in the past and the new architectural implementation is going on in the prospective of minimization of power, cost and area. This is because of digitization and the increase in demand of mobile computing devices.

To get high performance, semiconductor devices are shrinking to small sizes aggressively. This leads to increasing density of transistors on a die, higher frequency of operation and causing high power consumption. Source voltage is in balance and conserves it within limits to reduce power consumption, but the scaling of source voltage is restricted due to performance consideration. To address this issue we have to work on circuit techniques and system level design. [11]. Power consumption is a critical design issue in embedded processor design. One of common components in the processor is the Arithmetic and Logic Unit (ALU). ALU (arithmetic Logical Unit) called as the brain is most usable in any processor in the world. To design or implement a new processor totally depend on the Arithmetic logical unit.

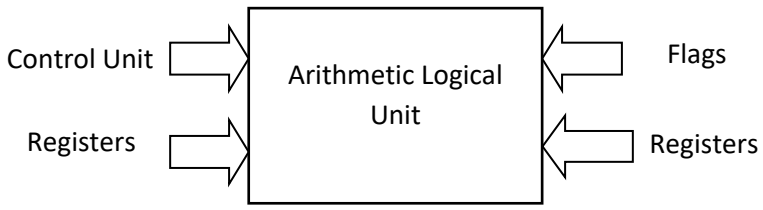

Figure1. Basic Arithmetic Logical Unit

ALUs are designed with a combinational logic, digital electronic circuit containing a number of functional components that performs arithmetic and bitwise logical operations on integer binary numbers. ALU operations are fixed and floating point operations. The figure shows the basic diagram of the arithmetic Logical Unit. If we can optimize activities on an ALU then power optimization issue can be solved.

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In this paper, we will study the concept and implementation of ALU design in detail. The different types of method, techniques and implementation of the ALU are explained in our paper. This paper is organized as follows: Section 2 present the Introduction, Section 3 describes the Literature survey of related work. Section 4 concludes this paper.

LITERATURE SURVEY

Andrew D. Booth et al. [1] design a method for A Signed Binary Multiplication. This technique is useful for a binary number multiplication, which is independent of the signs of these numbers. The automatic computing machines have advantages that multiplying of two numbers whose signs are not necessarily positive.

Libo Huang et al. [2] recommended the design of a low-cost binary 128 FMA unit with SIMD support. The proposed floating-point Fused multiply Add (FMA) design is executed a binary 128 FMA with two binary 64 FMA units. 64 FMA needs less hardware than a fully pipelined binary128 FMA. The implementation of the standard 128 FMA gives us 30 percent less area and 29 percent less dynamic power dissipation as compared to other design. This design method consumes significantly less area and power, whereas achieving improved performance for the applications with various floating-point precisions.

Abhishek Gupta et al. [3] implement an Arithmetic Logic Unit for efficient speed, energy and power. The proposed a speed, efficient multiplier and reversible logic gate. This proposed reversible logic gate does not only provide speed, efficiency, but also energy efficiency to the ALU, which directly affect the power efficiency. Along with this as our proposed design requires less area in logical unit which further makes ALU more power efficient. This Proposed Arithmetic Logical Unit is very useful for the Microprocessor/microprocessor and CPU whose performance is dependent upon the efficiency of the ALU. Proposed Multiplier can also be used for optimizing the MAC unit of DSP. Further, our proposed designs can also be used to optimize the different digital signal processing based algorithms such as FFT, FIR, and IIR etc.

Ruchir Guptel et al.[4] have proposed an interval based ALU with division by shifting is an implementation Architecture design have the use of a three stage pipelined multiplier. MA operator (multiply-accumulate) is implemented which reduced instruction set of addition, subtraction, multiplication, division. It can be also used for filtering operations. By reducing critical path, we improve the performance of the pipeline architecture. The results show that pipelined design operates at a maximum speed with minimum area. The presented technique for ALU shows significant improvement in throughput as compared to other design.

Yu Zhou et al.[5] implemented a VHDL customization approach for the low power ALU design. Many approaches are reducing power, but to achieve the power reduction, the complexity and cost of the design is increased which results as delay and area overheads. The experimental results show that ALU power reduction can be achieved. The approach is integrated using an HDL (Hardware Description Language).

Khaing Yin Kyaw et al. [6] define a new concept that involved accuracy as a design parameter. The techniques improve the performances of power consumption and speed. It is designed into the multiplication part and the non-multiplication part. MP is implemented using conventional method to certify a superior accuracy in the higher order bits while NMP is constructed in an innovative method that certificates positive quantity of errors. These multipliers are widely used in application specific data paths in multimedia and wireless communication applications. The degree of saturation error within the dynamic range of interest is tolerable depending of the level of perceptual quality and SN ratio degradation it induced.

Dimitri Tan et al. [7] describe Low-Power MPFPM with SIMD Support. MPFPM (Multiple-Precision Iterative Floating-Point Multiplier) technique completes the demand in the low-power computing market for a reduction in power consumption. The design of a well-matched FPM that is accommodating with the IEEE Standard for Binary FPA (Floating-Point Arithmetic). The other design has more area and more power dissipation as

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Impact Factor: 4.116
CODEN: IJESS7

compared to a proposed method. The design achieves improved performance because of design consumes less area and power. Also deliver good SIMD performance in a low-cost, low-power solution.

L. Sriraman [8] explains the novel multiplier architecture based on ROM approach using Vedic Mathematics. The architecture is similar to KCM (Constant Coefficient Multiplier). The projected multiplier is consuming less area and faster than other multipliers. It provides higher performance for higher order bit multiplication. This is mainly due to memory constraints. Effective memory implementation and deployment of memory compression algorithms can yield even better results.

Libo Huang et al. [9] implement a new technique floating-point MAF unit. The MAF (multiply-add fused) cares multiple IEEE precisions multiply-add process with SIMD feature. Each module of the outdated double precision MAF unit changed to multiple precision operations or repeating hardware properties when the module is on the critical data path. This method is extended to other floating-point operations, like multiple precision floating-point addition or multiplication for implementing SIMD instruction sets. The technique is speed up the floating point performance in technical and multimedia uses.

Rajit Ram Singh et al [10] describe ALU design and simulation in VHDL environment. The ALU design with pipelining delivers an extraordinary performance ALU to perform various instructions concurrently. To form a floating point ALU unit, we design four arithmetic modules which are addition, subtraction, multiplication and division. Each module is independent of other and further separated into sub-modules. The results achieved are suitable and are in accordance with theoretical expectations. Proposed design gives better performance as compared to the other conventional simulation method.

TABLE I: Summary of literature survey

Author	Method/Design/Implementation	Advantage
Andrew D. Booth et al. [1]	Signed binary multiplication	Multiplying of two numbers whose signs are not necessarily positive
Libo Huang et al.[2]	Low-cost binary 128 FMA unit with SIMD support	Less area and less dynamic power dissipation
Abhishek Gupta [3]	Multiplier and reversible logic gate	Speed, energy and power efficient
Ruchir Guptel [4]	Interval based ALU with division by shifting	Maximum speed with minimum area
Yu Zhou et al [5]	VHDL customization approach	Power reduction
Khaing Yin Kyaw et al.[6]		Improve the performances of power consumption and speed
Dimitri Tan et al [7]	Low-Power MPFPM with SIMD Support	Reduction in power consumption, consumes less area and deliver good SIMD performance.
L. Sriraman [8]	Multiplier architecture using Vedic Mathematics	Higher performance for higher order bit multiplication.
Libo Huang et al [9]	Floating-point MAF unit	Good performance in scientific and multimedia applications.
Rajit Ram Singh et al [10]	ALU design and simulation in VHDL environment	Better performance and less area

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CONCLUSION

In this paper various methods for ALU design has been reviewed. From the above literature we report different issues regarding the ALU design. Many approaches are reducing power, but to achieve the power reduction, the complexity and the cost of the design is increased which results as the delay and the area overheads.

REFERENCE

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[4] Ruchir Guptel et al. Pipelined ALU for Signal Processing to Implement Interval Arithmetic
[5] Yu Zhou et al. Application Specific Low Power ALU Design
[6] Khaing Yin Kyaw et al. Low-Power High-Speed Multiplier for Error Tolerant Application
[7] Dimitri Tan et al. Low-Power Multiple-Precision Iterative Floating-Point Multiplier with SIMD Support
[8] L. Sriraman et al. Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics
[9] Libo Huang et al. A New Architecture for Multiple-Precision Floating-Point Multiply-Add Fused Unit Design
[10] Rajit Ram Singh et al. VHDL environment for floating point Arithmetic Logic Unit - ALU design and simulation
[11] Kaushal Kumar Sahu SPAA aware error tolerant 32 bit arithmetic and logical unit for graphics processor unit